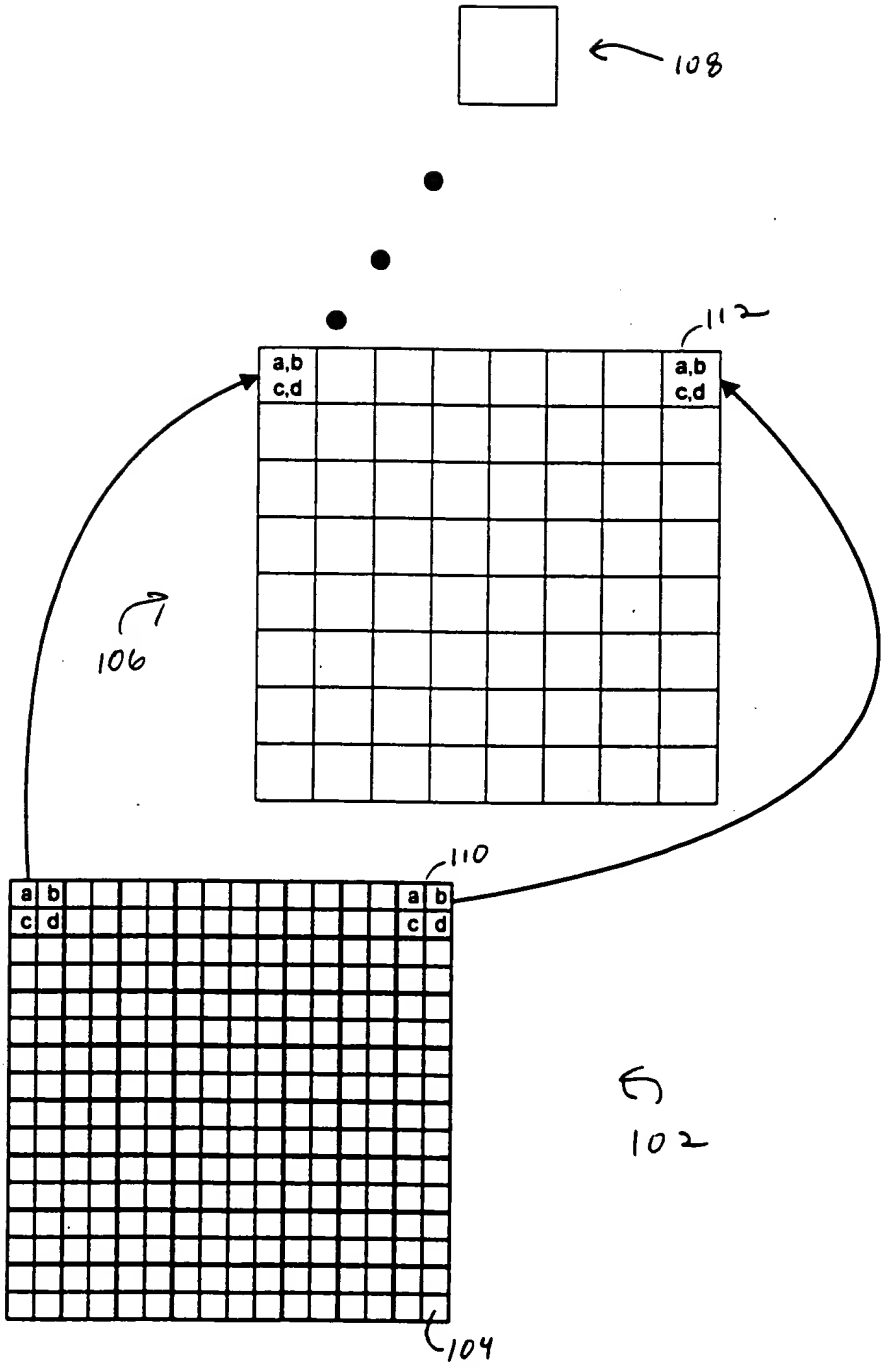

Figure 1

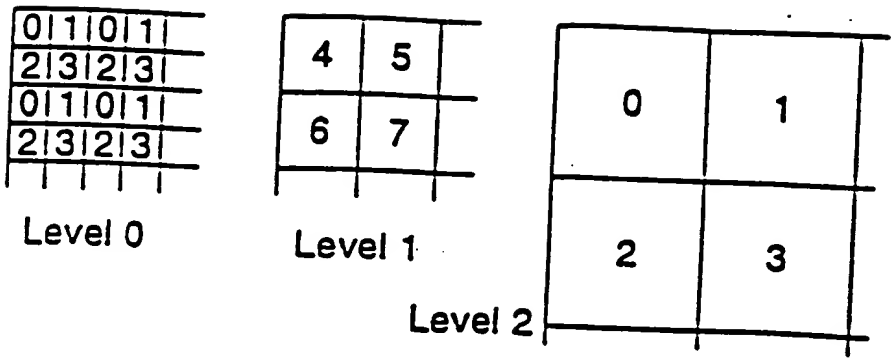

Figure 2

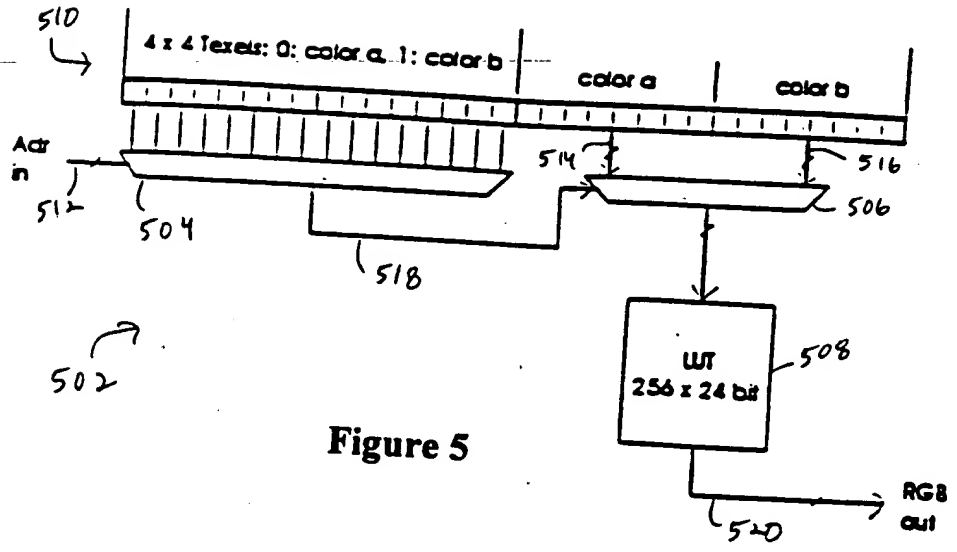

Figure 5

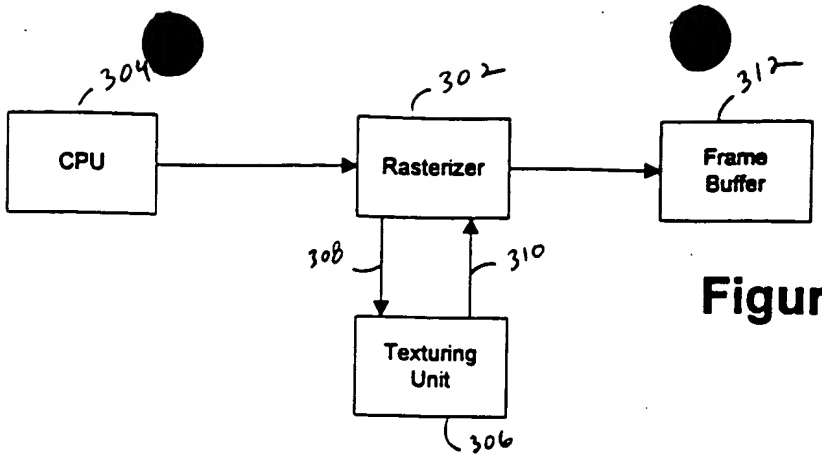

Figure 3

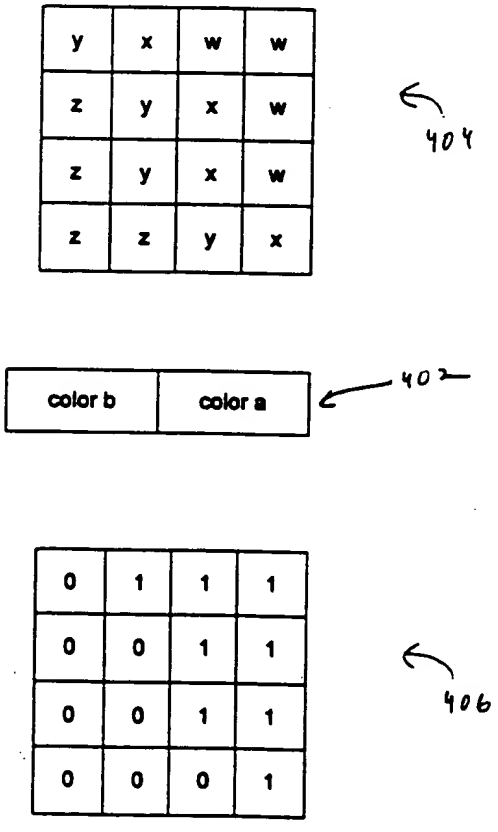

Figure 4

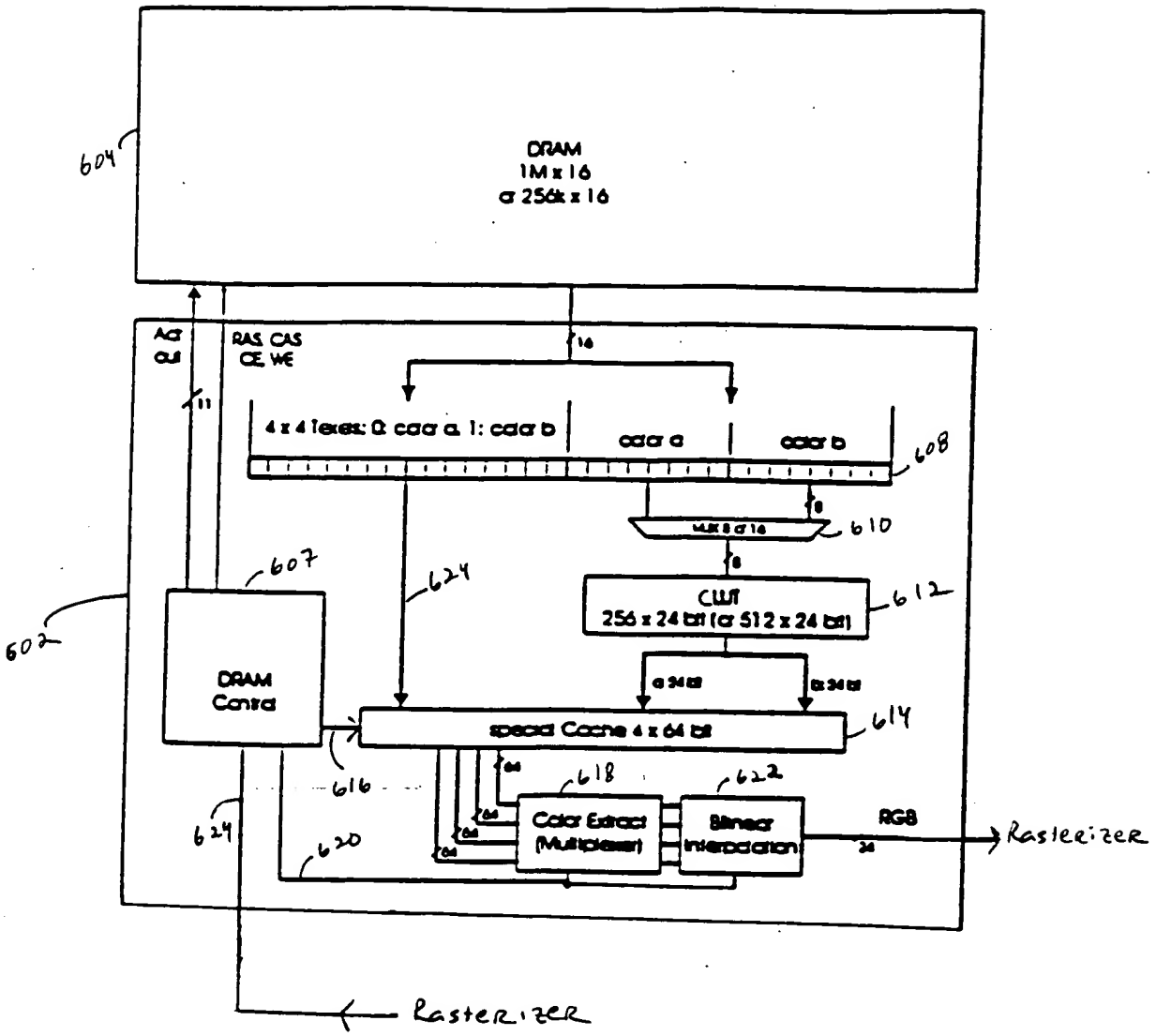
DRAM
1M x 16
or 256k x 16
604
RAS CAS
OE WE
16
11
4 x 4 Texels: 0: color a, 1: color b
color a
color b
608
8
610
607
624
602
CLUT
256 x 24 bit (or 512 x 24 bit)
612
DRAM
Contrl
Special Cache 4 x 64 bit
614
616
618
622
624
620
Color Extract
(Multiplexer)
Bilinear
Interpolation
RGB
24
Rasterizer
Rasterizer

Figure 6

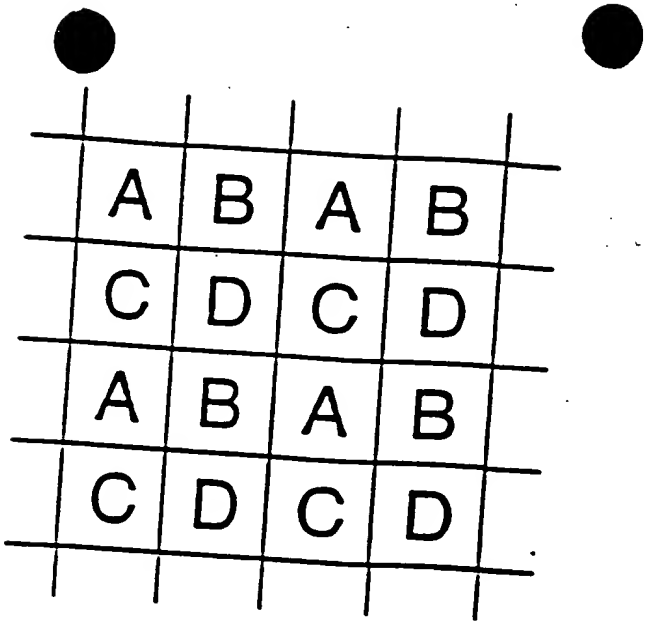

Figure 7

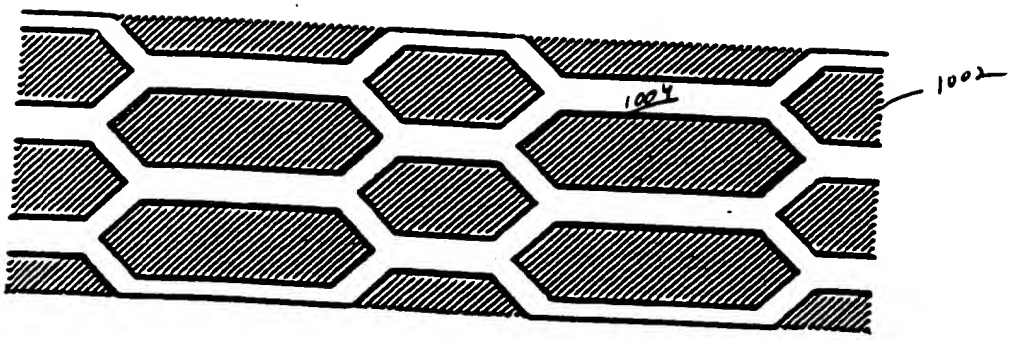

Figure 10

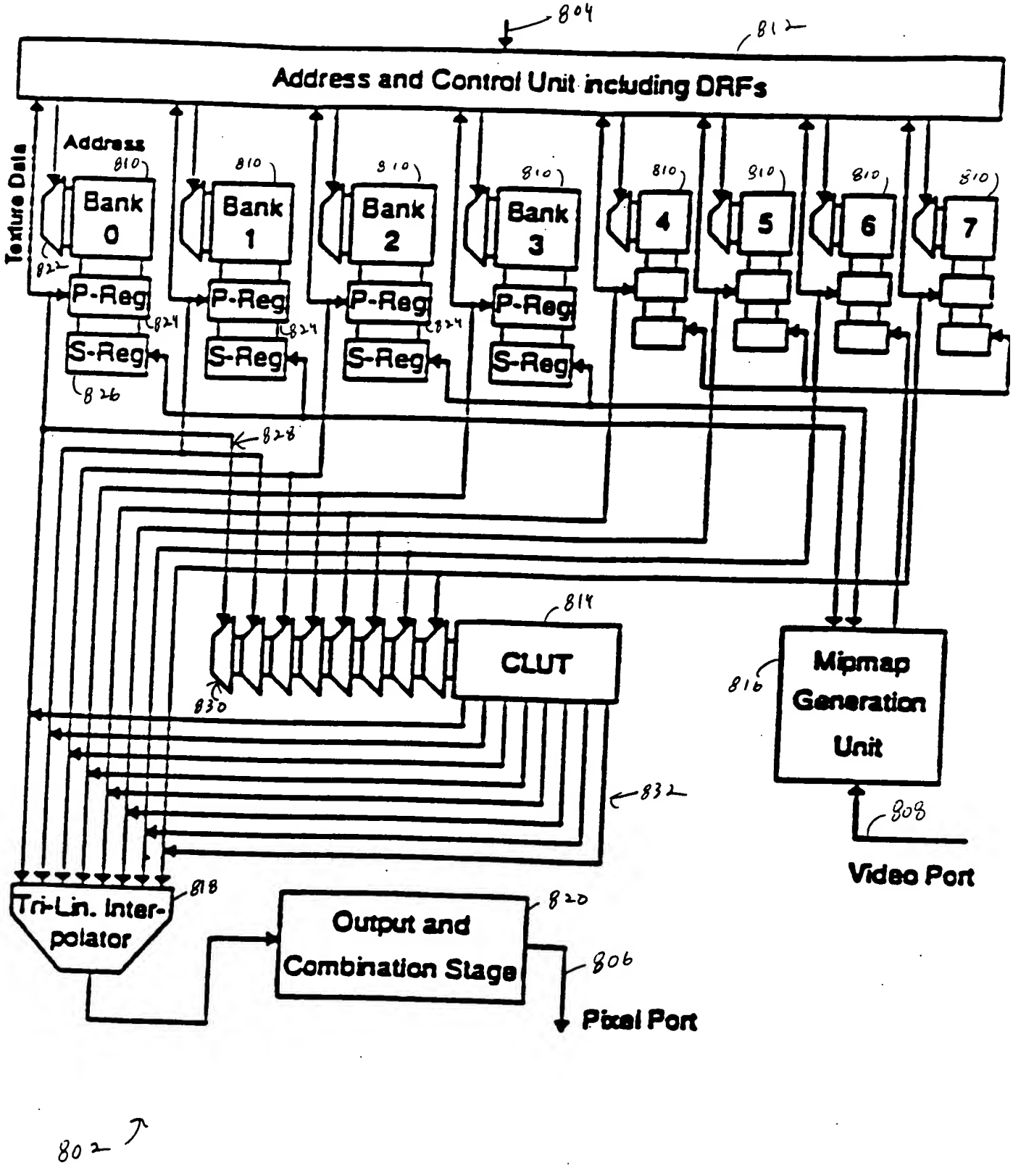
804
812
Address and Control Unit including DRFs
Texture Data
Address
810
Bank 0
Bank 1
Bank 2
Bank 3
4
5
6
7
822
P-Reg
S-Reg
824
826
828
814
CLUT
830
816
Mipmap Generation Unit
808
Video Port
832
818
Tri-Lin. Inter-polator
820
Output and Combination Stage
806
Pixel Port
802

Figure 8

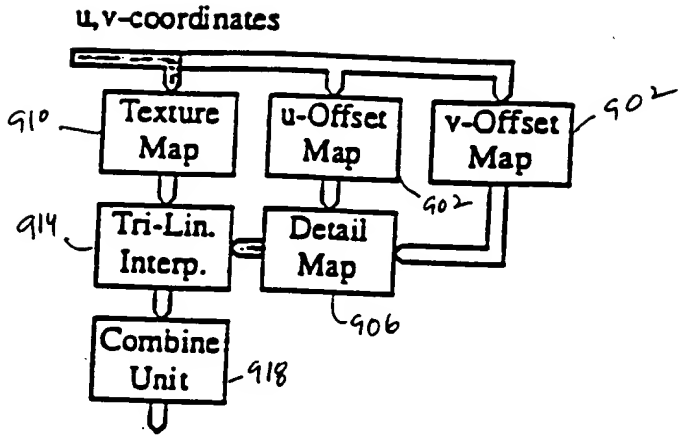

Figure 9(a)

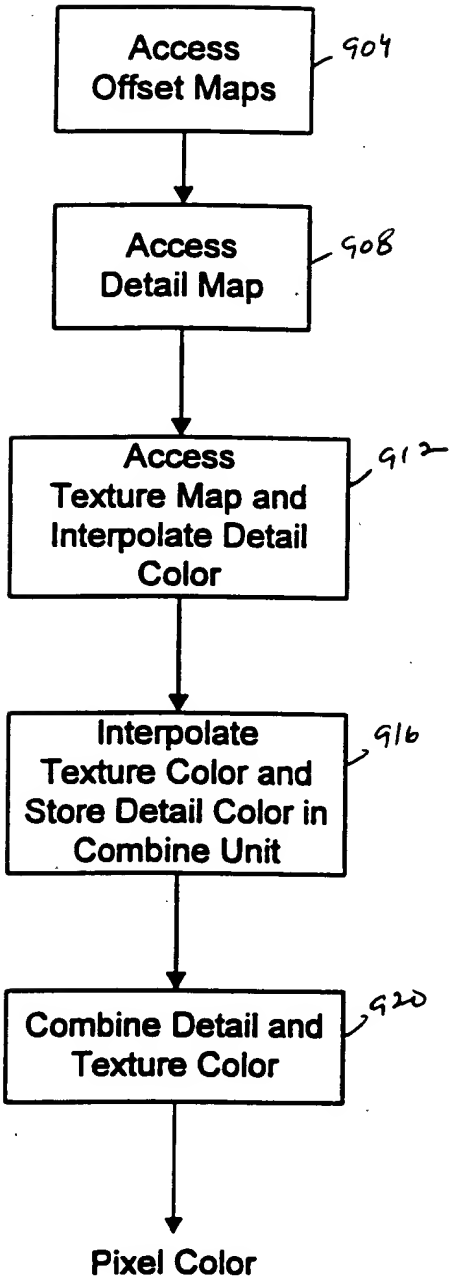

Figure 9(b)

09/09/2004 09:09:09

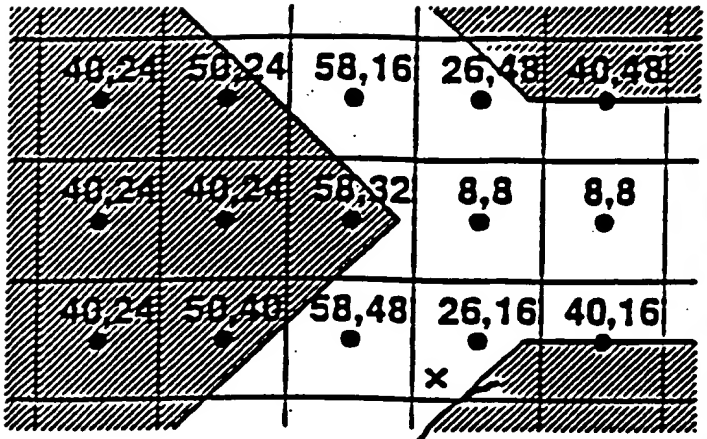

Figure 11(a)

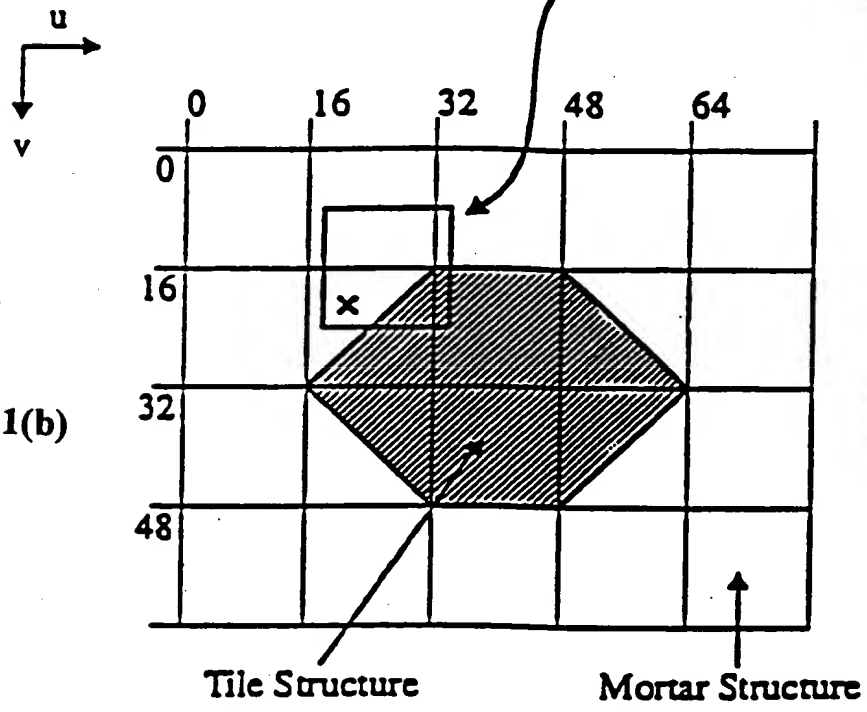

Figure 11(b)

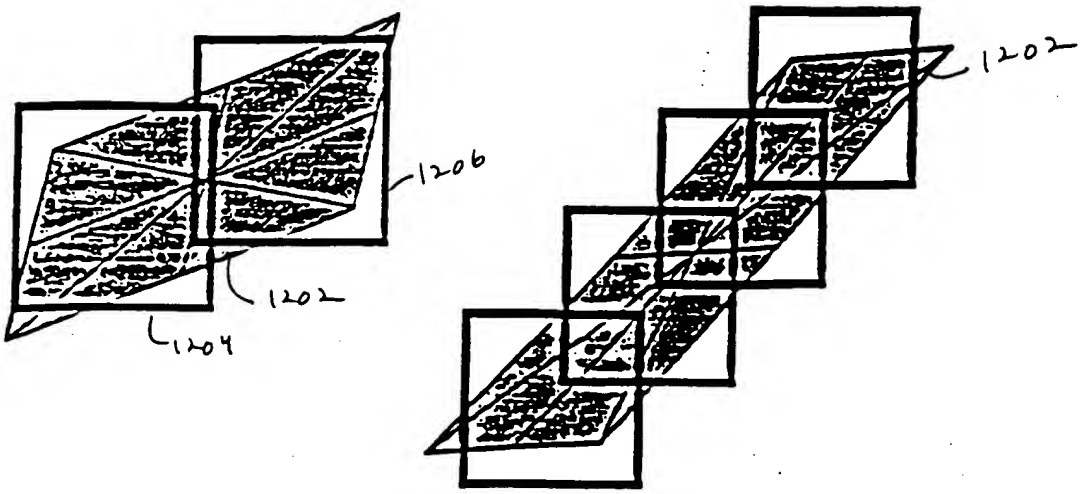

Figure 12

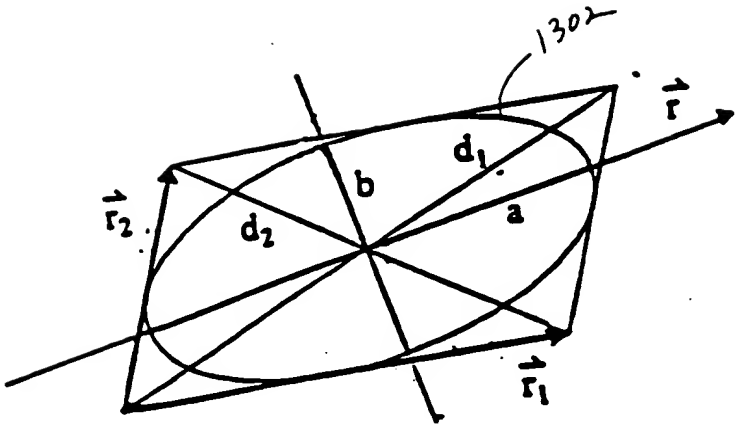

Figure 13

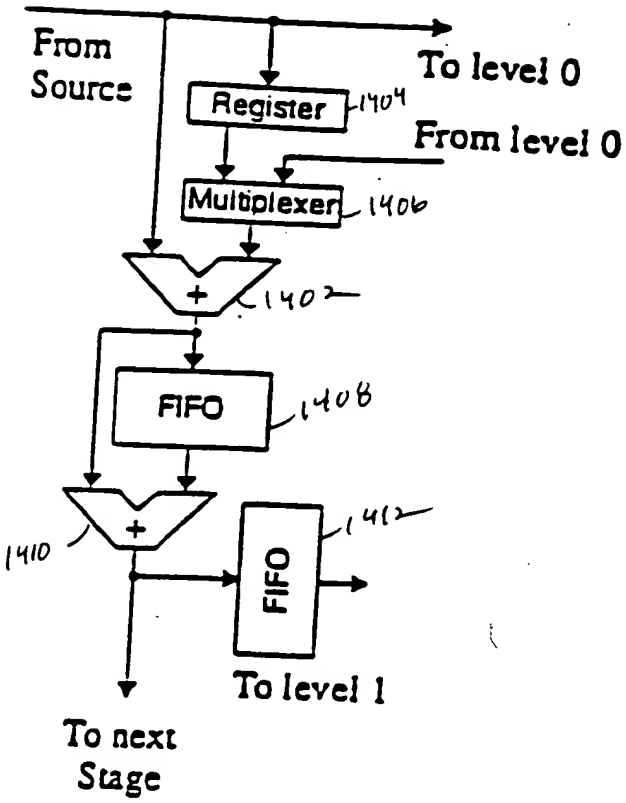

Figure 14(a)

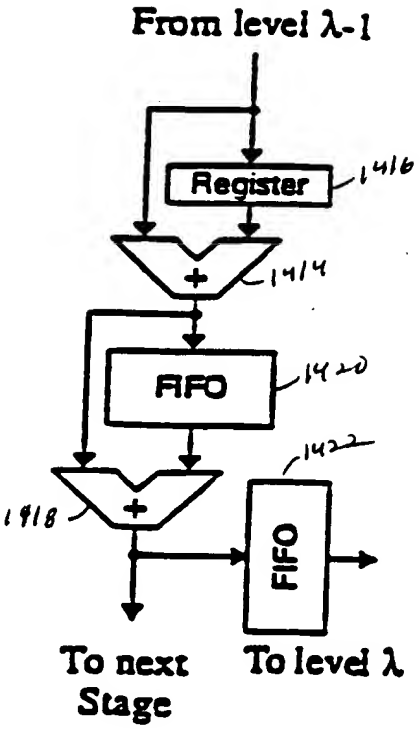

Figure 14(b)

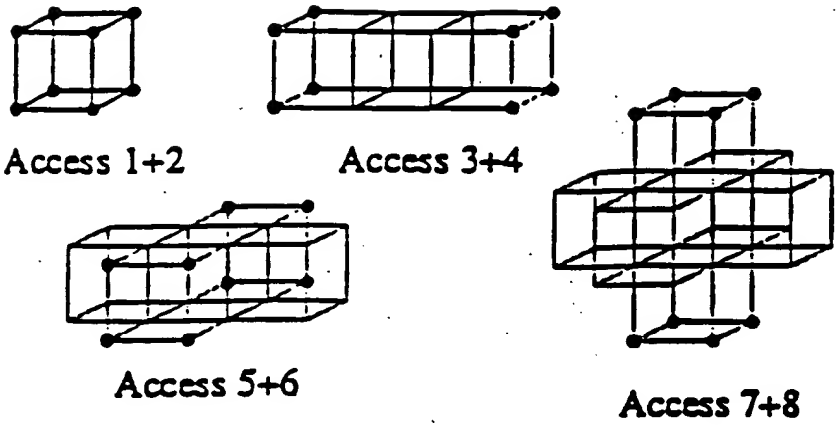

Figure 15

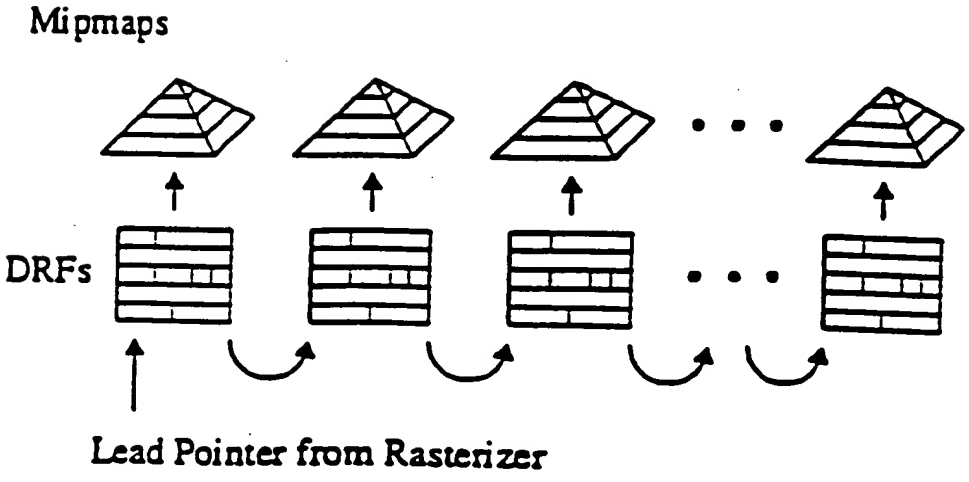

Figure 16